Thermal evaluation of metalized ceramic substrates for use in next- generation power modules toward international standardization

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***Abstract*— Wide bandgap (WBG) semiconductors such as SiC and GaN have opened their market as the next generation of high power modules. As advanced electronic power modules must deal with increasing power density, power modules with an insulating ceramic substrate are subjected to extremely high temperature due to high current and voltage. Currently, the junction temperature of Si power devices is kept low enough, around 150 ℃, to maintain the module durability. Nevertheless, the temperature will be soon beyond 200 ℃ for WBG devices. Thus thermal dissipation performance has one of the key technologies in designing modules. Directly bonded copper (DBC) or aluminum (DBA) substrates have been widely used as two of the typical ceramic insulating substrates for high power modules. If the extensive heat from a junction is kept inside a module, the module will be easily damage due to the increasing temperature resulting in severe thermal stress inside. Designing a proper module structure requires not only each material property but also complex component shape/structure/layout including each interface heat transfer. An accurate measurement method of precise thermal properties for such a complex metallized ceramic substrates is currently still missing. To meet the urgent requests for the next generation of high power modules, a new and simple measurement method of the thermal properties has been proposed for complex metallized ceramic substrates. First we have designed a micro heater SiC chip as an accurate and controllable heat source instead of a SiC active die. The heater chip was die-attached on metallized ceramic substrate mimicking real module packaging structure. The thermal resistance of the metallized ceramic substrate was evaluated. Due to the high power of the chip, i.e. 1 kW/cm^2, the obtained thermal resistance has an excellent accuracy within a few percent error, when adequate cooling system is used. The thermal resistance includes those of die-attach material and thermal interface materials (TIM). The developed method thus enables precise comparison in thermal properties of high power modules, which was proposed as an ISO standard.**

Keywords— Thermal resistance, SiC, Power module, DBC/ AMB substrate, Thermal interface material (TIM).

Ⅰ. INTRODUCTION

Recently, the next-generation power devices have rapidly been developed using semiconductors such as SiC or GaN. However, the downsizing of the modules with highly increased power density causes increased and concentrated heat generation from electric conversion loss. The thermal management thus becomes more important for realizing high reliability and longer life-time of the power devices. In a power module, the heat produced by a semiconductor element spreads through substrates, bonding wires and the mold or insulating materials [1]. Hence the metal bonded ceramic substrates are often used for high power devices to decrease the thermal resistance between the device chips and the cooling system, while a high thermal conductivity is required for the substrate. For such ceramic substrate materials, Al_2O_3 has been adopted though its thermal conductivity is low as 30 W/(m·K). Ceramics made of AlN has high thermal conductivity about 180 W/(m·K), but the mechanical properties are often regarded as insufficient to assure the device reliability. Recently, silicon nitride (Si_3N_4) has attracted much attention as a ceramic substrate because of the improved thermal conductivity achieving 90 W/(m·K) with excellent mechanical properties.

In accordance with the substrate developments, die-attach materials are also required high thermal performance. Ag sinter bonding is hence emerging as a replacement of Pb-Sn solders, which has traditionally been used for power devices, with the remarkable thermal conductivity as well as superior thermal stability at high temperature operations [2-6]. These properties of Ag sinter die-attach are suitable for wide-bandgap semiconductors, and thus advanced high power modules are designed with Ag sinter bonding combined with the advanced substrate materials mentioned above. However, accurate evaluation method of the thermal resistance in an assembled state for such a module has not yet established, mainly due to the difficulty to measure the high thermal conductivity through thin composite layers usually less than 1 mm.

To meet the above requirements, we have examined a method for evaluating thermal performance of a simplified device model, which consists of a SiC micro heater chip with temperature sensor bonded on a metalized ceramic substrate. The micro heater chip mimicking a high power device has been developed particularly for simulating heat generation by a SiC device [7-9]. As a first stage of investigation, we here measure the effective heat resistance between the micro heater chip and cooling plate, modeling a typical module structure where Si_3N_4 substrate with Cu layers bonded by active metal brazing (AMB), and Ag sintering die-attach. Two types of Cu metalized Si_3N_4 substrates with different circuit patterns were employed. Thermal resistance and warpage of each pattern were investigated. The results indicate that our method can characterize the heat spreading through various metalized ceramic substrates.

II. Experimental

A. *The resistance measurement principle for metalized ceramic substrate*

A *n*-doped 4H SiC single crystal wafer was cut to SiC-TEG chips (5 mm × 5 mm × 0.35 mm), which is commonly used for SiC devices, is adopted to fabricate the micro heater chip as shown in Fig. 1. A thin alumina layer is deposited on the wafer surface for insulation, and then Pt thin films are formed for both heater and temperature probe by lithography. Electric power as shown in Eq. (1) can be applied to the chip for Joule heating at maximum 250 W, where I and V denote heater current and voltage, respectively.

Two types of Cu metalized Si_3N_4 substrates with the two different circuit patterns were employed as shown in Fig. 2 (a) and Fig. 2(b), respectively. The former has a small metal pad with 7 mm square for die-attachment at the center surrounded by four electrode pads (afterward call that pattern a). The latter is composed of a large area of the metal pad for chip bonding with four small electrode pads at the substrate corners (afterward call that pattern b). The backside of the both substrate types are metalized with Cu plate of almost the same size as the ceramic plate.

In addition, as a die attach material, micron size Ag flake and spherical submicron Ag particles (Senju Metal Co., Ltd, Japan) were mixed for use as the Ag filler of pastes at a weight ratio of 1:1. These hybrid particles were then stirred magnetically for 10 min and vibrated ultrasonically for 30 min with viscosity of 100 ~ 200 Pa·s solvent using a hybrid mixer (HM-500, Keyence Corporation) to fabricate Ag paste to achieve a uniform mixture. The amount of solvent was maintained at approximately 10 wt% in the paste to maintain a suitable viscosity of 150-250 cPs at room temperature. For bonding to the DBC substrates, 100 nm Ti and 2 μm Ag were sputtered on both the back side of TEG-SiC chip and on the top side of the AMB substrates. Ag and Ti layers acted as an adhesion layer and diffusion barrier, respectively. The printing and sintering process of Ag sinter joining to substrate are introduced in our previous studies [10,11]. After die-attached by Ag sinter joining, the SiC-TEG chips was wire bonded at the Au electrode (see Fig.1) to AMB substrate. Fig.3 (a) and Fig.3(b) show the SEM image of Au wires and its magnified view, respectively. The die-attached structure was then bonded with a cooling plate by TIM.

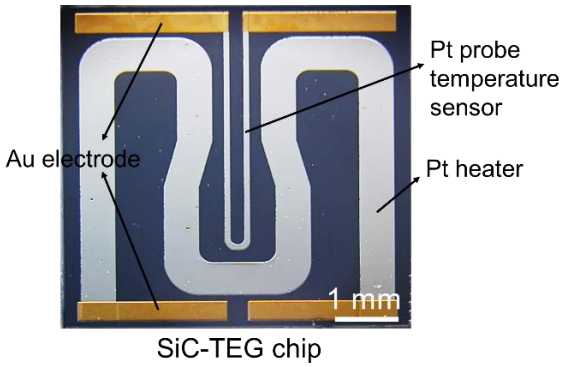

Fig. 1. The schematic diagram of equipment and measurement principle of the steady-state method

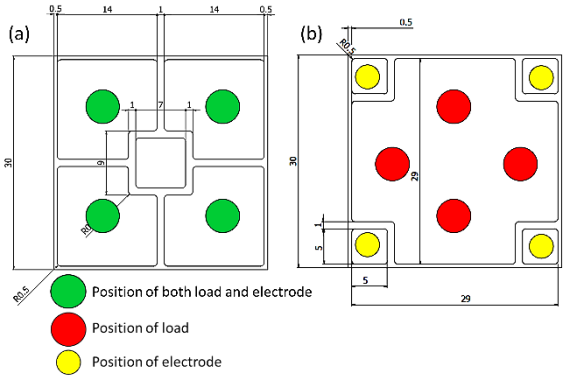

Fig.2(a) Circuit pattern ***a*** of a specimen substrate, (b)Circuit pattern ***b*** of a specimen substrate

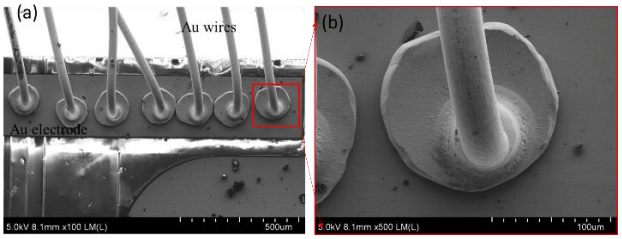

Fig.3(a) the SEM image of Au wires bonded at the Au electrode and (b) its magnified view.

The generated heat on the chip is transferred to the water cooling plate through the metalized ceramic substrates, and the heat is dissipated by external cooling system. Fig.4 illustrate the power cycling test systems applied the SiC-TEG chip and its integration into a minimized test package. The developed systems are consisted three major parts for power supplier, system controller and test plate. This system is used in controlled by an algorithm built with the python language to implement precise ON/OFF switching in real time, and the water-cooling system is maintained at 25 °C and the temperature between a substrate and a heat sink plate is measured by thermocouples during the operation. The condition of power cycling test was applied 2 seconds ON and 5 seconds OFF up to maximum 200 W(I = 2 A and V $\leqslant$ 110 V) repetitive. At this time, the temperature gradient, ΔT is occurred between the TEG chip surface of

joule heating and bottom of metallized substrate. The temperature gradient equation is given by:

$$\Delta T = T_{\text{chip surface}} - T_{\text{bottom of substrate}} \quad (1)$$

When the system reaches steady state, i.e. both the temperatures of heater chip and surface of the cooling plate become stable, the heat resistance, R_{th}, of the substrate can be calculated as the Eq.2, where ΔT is the temperature deference between the heater chip and the surface of the cold plate, and Q is the applied electric power. Note that the accuracy of R_{th} mainly depends on that of ΔT so that special care should be taken for the temperature measurements.

$$R_{th} = \Delta T / Q \quad (2)$$

The temperatures of the heater and probe are calculated from the electric resistivity of Pt wire that shows linear temperature dependence. Thus the change of thermal resistance can be monitored during the power cycle tests by use of this system.

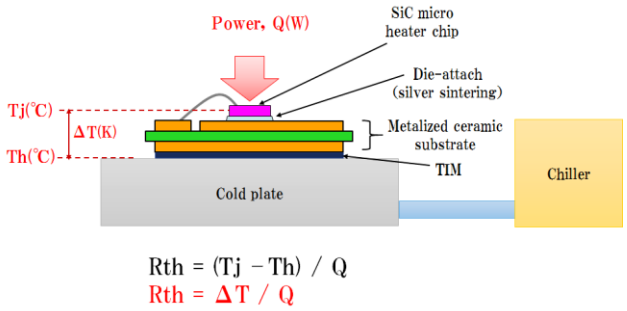

Fig. 4. The structure of SiC micro-heater chip

III. RESULTS AND DISCUSSION

A. *Ag sinter joining*

Fig. 5(a) and Fig. 5(b) show the cross-section of the SiC-TEG chip die-attached structure by Ag sinter joining and its magnified view at the bonding interface between Ag sinter layer and AMB substrate, respectively. The sintered Ag paste exhibited a micron-sized porous structure with Ag particles causing by Ag necking growth. The bonding interfaces between sintered Ag paste and AMB substrate suggested that sintered Ag paste tightly adheres to the AMB substrate by interface necking growth and inter-diffusion with Ag metallization.

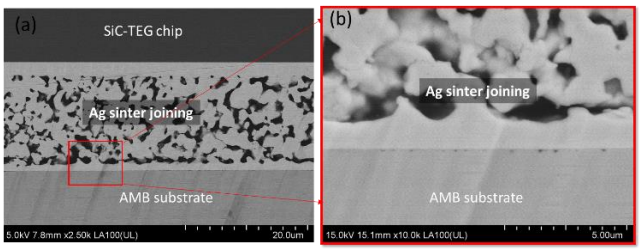

Fig. 5(a) the cross-section of the SiC-TEG chip die-attached structure by Ag sinter joining and (b) its magnified view at the bonding interface.

B. *Thermal resistance of metalized ceramic substrates*

During each R_{th} measurement, 10 kg·f load was applied to the metalized ceramic substrate specimen by the four metal pad to ensure the sufficient adhesion and thermal contact between the specimen and the cooling plate as shown in Fig.4. Then, R_{th} of the specimens were recorded for four different electric powers Q value, and repeated for several times. The different Q lead to a different ΔT. The maximum ΔT was about 171℃ and the minimum was about 45℃. For the circuit pattern ***a,*** the results of heat resistance are shown in Fig. 6. The larger ΔT shows a larger value of heat resistance, and the value of heat resistance shows a decrease trend with the increased repetition times and convergence after three times.

Fig. 7 shows the results of heat resistance measured for the circuit pattern ***b***, which shows the similar trend as introduced as circuit pattern ***a.*** However, the heat resistance of pattern ***a*** is generally higher (about 0.1 K/W) than those for the pattern ***b*** due to the limited heat spreading in the first Cu layer, and tends to decrease with increasing number of measurements. On the contrary, R_{th} for pattern ***b*** remains stable during the repeated measurements. One possible reason of low and stable R_{th} achieved by the pattern ***b*** specimen can be explained by the symmetric structure between metal patterns of front and back side, while asymmetric pattern ***a*** specimen causes warpage by various heating processes. Fig. 8(a) and Fig.(b) shows the 3D image of warpage for pattern ***a*** and pattern ***b*** after heat process, respectively. The warpage of the pattern ***a*** during the power on-off exchange was achieved about 50 μm, but the warpage for the pattern ***b*** almost did not warpage happen. The result can be clearly seen in Fig. 8(c) and Fig.(d), which are the height plot in the middle line of the pattern ***a*** and pattern ***b***, respectively. Therefore, the warpage will happen during the power cycling test, which largely depends on the design of Cu pattern. In addition, the warpage of the AMB substrate also influences the measurement of the heat resistance for the SiC power modules.

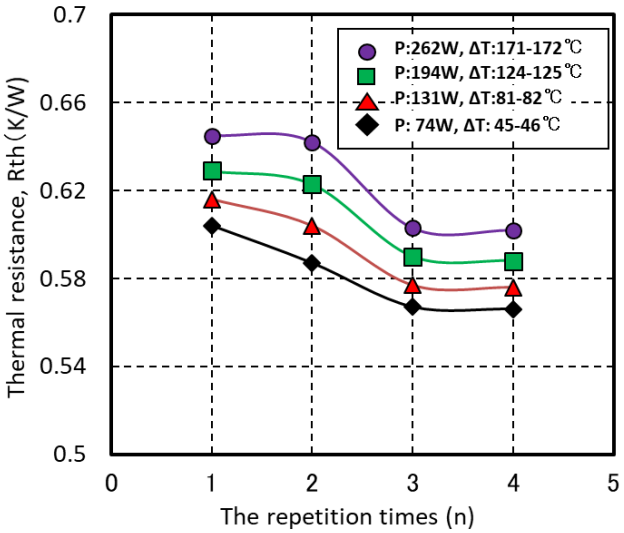

Fig. 6 Measured thermal resistance of metalized ceramic substrate with circuit pattern ***a***

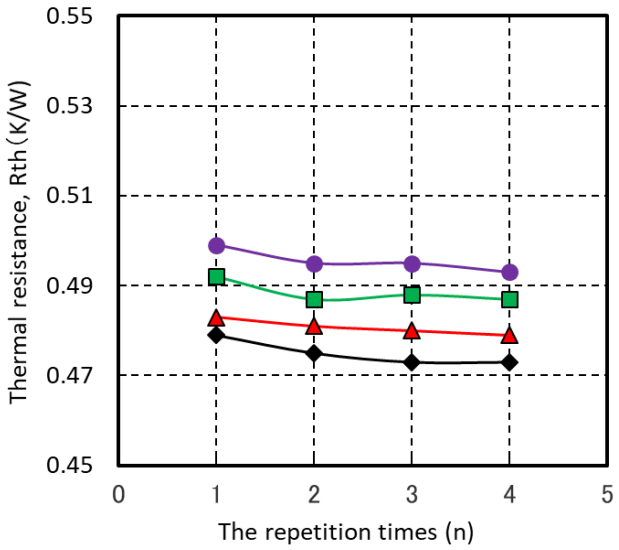

Fig. 7 Measured thermal resistance of metalized ceramic substrate with circuit pattern ***b***

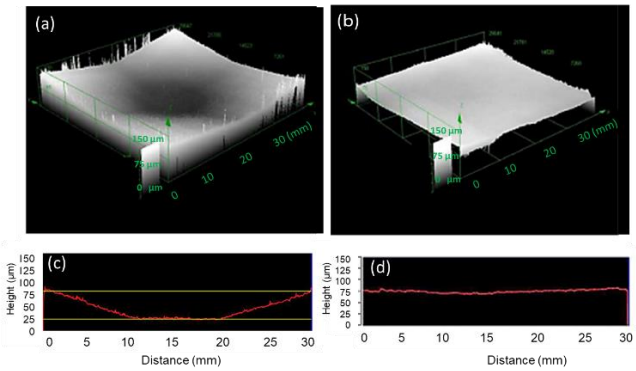

Fig. 8 (a) the 3D image of warpage for pattern ***a*** and (b) pattern ***b*** after heat process,(c) the height plot in the middle line of the pattern ***a*** and (d) pattern ***b.***

Ⅳ. CONCLUSIONS

In this study, we have demonstrated that accurate measurements of heat resistance R_{th} of metalized ceramic substrates can be achieved by using SiC micro heater chip equipped with a temperature probe, modeling a typical module structure where Si_3N_4 substrate with Cu layers bonded by active metal brazing (AMB), and Ag sintering die-attach. Two types of Cu metalized Si_3N_4 substrates with different circuit patterns were employed. Thermal resistance and warpage of each pattern were investigated. The larger ΔT shows a larger value of heat resistance, and the value of heat resistance shows a decrease trend with the repetition time. In addition, the warpage will happen during the power cycling test, which depends on the design of Cu pattern. The warpage also influences the measurement of the heat resistance for the SiC power modules. The method developed here would be proposed for ISO standardization, to serve the effective thermal characterization of various metalized ceramic substrates usable for advanced power electronic module designs.

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REFERENCES

[1] N. Wakasugi, S. Nagao, K. Takeshita, D. Kim, A. Shimoyama. N. Satou, K. Suganuma, “Thermal characterization of metal bonded ceramic substrate by power cycling test using SiC heater chip,” The 33rd Conference of JIEP, Bunkyo Campus, Takushoku University, JAPAN;11-13 March, 2019.

[2] C. Chen, C. Choe, Z. Zhang, D. Kim, K. Suganuma, Low-stress design of bonding structure and its thermal shock performance (-50 to 250 °C) in SiC/DBC power die-attached modules, J. Mater. Sci. Mater. Electron., 29 (2018) 14335-14346.

[3] Z. Zhang, C.Chen,Y.Yang, H. Zhang, D. Kim, T. Sugahara, S.Nagao, K.Suganuma, Low-temperature and pressureless sinter joining of Cu with micron/submicron Ag particle paste in air, J. Alloys Compd., 780 (2019) 435-442.

[4] C. Chen, S. Nagao, K. Suganuma, J. Jiu, T. Sugahara, H. Zhang, T. Iwashige, K. Sugiura, K. Tsuruta, Macroscale and microscale fracture toughness of microporous sintered Ag for applications in power electronic devices, Acta Mater., 129 (2017) 41-51.

[5] C. Chen, K. Suganuma, T. Iwashige, K. Sugiura, K. Tsuruta, High-temperature reliability of sintered microporous Ag on electroplated Ag, Au, and sputtered Ag metallization substrates, J Mater Sci: Mater Electron., 29 (2018) 1785-1797.

[6] C. Chen, K. Suganuma, Microstructure and mechanical properties of sintered Ag particles with flake and spherical shape from nano to micro size, Mater. Des., 162 (2019) 311-321.

[7] N Wakasugi, S Nagao, D. Kim, K Suganuma, “High heat-density SiC heater chip for thermal characterization of high temperature packaging,” IMAPS High Temperature Electronics Conference (HiTEC), Albuquerque, NM, United States; 8-10 May 2018.

[8] D. Kim, S. Nagao, N. Wakasugi, Y. Yamamoto, A. Suetake, T. Takemasa, K. Suganuma, “Power cycle tests of high temperature Ag sinter die-attach on metalized ceramic substrate by using micro-heater SiC chip,”51st International Symposium on Microelectronics, (IMAPS 2018), Pasadena, CA, United States; 8-11 Oct. 2018.

[9] D. Kim, Y. Yamamoto, S. Nagao, N. Wakasugi, C. Chen, K. Suganuma Measurement of Heat Dissipation and Thermal-Stability of Power Modules on DBC Substrates with Various Ceramics by SiC Micro-Heater Chip System and Ag Sinter Joining, Micromachines 10 [11] (2019)745-755.

[10] D. Kim, C. Chen, S. Nagao and K.Suganuma, Mechanical characteristics and fracture behavior of GaN/DBA die-attached during thermal aging: pressure-less hybrid Ag sinter joint and Pb–5Sn solder joint. J Mater Sci: Mater Electron, 31 (2020) 587–598.

[11] D. Kim, C. Chen, S. Noh, S-j. Lee, Z. Zhang, Y. Kimoto, T.Sgahara and K. Suganuma, Development of high-strength and superior thermal shock-resistant GaN/DBA die attach structure with Ag sinter joining by thick Ni metallization, Microelectron Reliab, 100–101 (2019), 113380.